REMARKS

This amendment responds to the office action mailed March 13, 2006. In the office action the Examiner:

- allowed claims 9-24;
- object to claim 25 for containing informalities;
- rejected claims 2-4, 6 and 25 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Olarig et al (US 6,449,677) and Harriman (US 6,330,645);
- rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Olarig et al (US 6,449,677) and Harriman (US 6,330,645) and Lo et al. (US 6,115,760);
- rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Olarig et al (US 6,449,677) and Harriman (US 6,330,645) and Takada et al (US 6,633,961)

After entry of this amendment, the pending claims are: claims 2-25.

Overview of Changes to Claims

Claim 25 has been amended to overcome the formalities objection. No new matter has been added.

35 USC 103(a) Rejections

In the Office Action, the Examiner has rejected claims 2-4, 6 and 25 as being unpatentable over Butler, Olarig, and Harriman. The Applicants respectfully disagree and traverse.

Notes: Video capture board 214 of Butler does not control the system memory 206. It simply dumps video data to a bus 212, and then other devices move the data from the bus 212 to the system memory 206.

Butler does not Teach the Basic Elements of Claim 2

As will be explained next, Butler does not teach the basic elements of claim 2. As an initial point, it is noted that the Examiner's explanation concerning Butler with respect to claim 2 is inconsistent with respect to the "memory device" and the "buffer" elements of claim 2. On the one hand the Examiner identifier system memory 206 of Butler as the

memory device element, but in the explanation of the buffer control logic the Examiner identifies SDRAM buffer 306 as the memory device. This inconsistency makes the Examiner's explanation difficult to follow.

More importantly, the controller 304 of Butler is not a memory controller for the system memory 206. For instance, the controller 304 of Butler is incapable of performing a read operation against the system memory 206. The entire purpose of the video capture board 214, of which controller 304 is one component, is to stream video data onto an internal bus 212. From the bus 212, the video data is stored in system memory 206. But the video capture board 214 and its memory controller 304 are incapable of issuing read commands to the system memory 206 (as required by all the pending independent claims of the present application).

Secondly, and this is very important, the only memory from which the controller 304 reads is the SDRAM buffer 306. Furthermore, the description in the last paragraph of column 6 in Butler makes clear that read operations by the controller 304 never use the same address as the address for a pending write operation. This is because the read operation is enabled only after the video data has been written into the SDRAM buffer 306.

As a result, the memory controller 304 of Butler does not "delay[s] issuance of the read command to the memory device" because (a) the memory controller 304 never sends any read commands to the system memory 206, and (b) the memory controller 304 is incapable of having a read command use the same address as a pending write command. In addition, the Examiner has not cited either Olarig or Harriman as having the basic elements of the pending independent claims. For these reasons, all the pending rejections under 35 USC 103(a) should be withdrawn.

There is No Motivation to Combine Harriman with Buttler/Olarig

The Examiner has argued that there is motivation for combining the teachings of Butler, Olarig, and Harriman in a manner that achieves the claimed combination of claim 2:

> Regarding claim 2, it would have been obvious to one of ordinary skill in the art, having the teachings of Butler and Olarig and Harriman before him at the time the invention was made, to modify the system of Butler and Olarig to include the controller performs [sic] delaying a read command when an address corresponding to the read command is the same as the first address because it would have provided **needed coherency** by reducing the average performance cost of the coherency

scheme (col. 2, lines 27-28) as taught by Harriman. (emphasis added)

The applicant disagrees that combining the teachings of Harriman with those of Butler and Olarig is motivated by these references, as will be explained below.

From the perspective of the Butler reference, which is the primary or foundation reference cited by the Examiner, the video data storage memory in a video acquisition system is an unlikely candidate for applying the memory coherence logic of Harriman. There is, in fact, no need for memory coherency control in Butler. The simple logic represented in Figure 5 of Butler addresses transaction ordering, but the sole purpose of this ordering logic is to ensure that an internal buffer with high priority data does not overflow – which would cause the permanent loss of data by the video acquisition system. Butler has no other need for transaction ordering because the Butler system is incapable of suffering from memory coherency problems. There are no transactions or operations described in Butler that would cause a memory coherency problem. For this reason, the Examiner's statement, quoted above, concerning "needed coherency" is incorrect. There is no "needed coherency" in the Butler system.

It is further noted that the teachings of Olarig are combined by the Examiner with those of Butler solely for the purposes of addressing the "pipelined" read and write commands aspect of claim 2. Therefore the "system of Butler and Olarig" has no more need for coherency logic than the Butler system.

For these reasons, the applicant requests that the Examiner withdraw all rejections under 35 U.S.C. 103 that rely upon a combination of the Butler and Harriman references.

In addition, it is noted that the invention claimed in claim 2 concerns the processing of pipelined memory access commands. A person of ordinary skill in the art would not look to teachings concerning memory coherence for multi-processor or multi-user systems while designing a memory controller that processes pipelined memory access commands. The coherency control 228, arbiter 224, snoop control (Fig. 3a) and other aspects of Harriman for determining when to delay the execution of memory commands are irrelevant to the controller of claim 2, which has an interface for receiving pipelined read and write commands. There would be no reason to use the complicated memory coherency circuitry of Harriman in the context of the invention claimed in claim 2, and therefore there is no motivation to combine Harriman with Butler and Olarig.

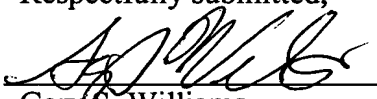
Thus, the memory coherence logic and teachings of Harriman are irreconcilable with the invention defined by claims 2 and 25, and their dependent claims. For these additional reasons, the applicant requests that the Examiner withdraw all rejections under 35 U.S.C. 103 that rely upon a combination of the Butler and Harriman references.

CONCLUSION

In light of the above amendments and remarks, the Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 15, 2006



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